

# HOT CHIPS 19



..... The annual Hot Chips symposium continues to attract good papers and an interested audience. For Hot Chips 19, we received 65 submissions, maintaining the record pace of the last few years, and once again, substantial discussion was needed to select papers for presentation from the large number of promising candidates. Hot Chips always tries to offer our attendees fresh technical information on important new chips and relevant technologies.

We selected papers ranging from interesting research efforts to new commercial products. We also made an increased effort to encourage authors to present design “insight” over data sheets, because past attendees have responded well to papers explaining how and why decisions were made. We included some chip-related software and evaluation content, since silicon alone is never enough.

As usual, we had high-end microprocessors, embedded and media processors, switch and networking chips, wireless chips, and memory technology. We continued last year’s emphasis on multicore chips, but added more content on the software necessary to make them work well, with multicore designs for general-purpose CPUs, graphics processors, and several other interesting new designs.

We had an especially diverse mix of panel sessions, keynotes, and a special presentation. These ranged from near-term product directions and technologies to consideration of much broader issues, and ended with a special presentation on wireless broadband and entrepreneurship by Reed Hundt. We included these in the symposium to give us all some broader context for the design, use, and future of chips—in addition to the low-level bits and bytes.

Our first tutorial, “Approaches to System Design for the Working Engineer,” addressed a real issue for many engineers, that of choosing among different kinds of system implementations—such as ASICs, application-specific programmable processors, and FPGAs—with varying trade-offs.

Our second tutorial, “Enterprise Power and Cooling: A Chip-to-Data Center Perspective,” was a systems-oriented, bottom-to-top discussion that certainly placed “hot chips” in context among the various “hot” things we now have.

We thank the Program Committee for its hard work. The PC issues the usual call for papers, but increases the available pool of presentations to be evaluated by chasing people known to be doing interesting things. Unlike most conferences, Hot Chips presentations are accepted on the basis of abstracts. The proceedings consists of copies of the speakers’ slides rather than full papers. This process enables all PC members to read all abstracts, and is sufficiently less time-consuming than the process for most conferences; the goal is to encourage key working engineers to submit presentations that are extremely up to date.

Although presentations are conditionally accepted via abstract, the session chairs must review, sometimes edit, and approve each set of slides. This process occasionally leads to “interesting” discussions among presenting engineers, marketeers, lawyers, and session chairs—especially for products that are just about to be announced. Presentations are available at [www.hotchips.org](http://www.hotchips.org), and you can find the Hot Chips 19 program at [www.hotchips.org/archives/hc19](http://www.hotchips.org/archives/hc19).

Finally, the PC selects “Best of Hot Chips” presentations, whose authors are invited to prepare actual papers for this

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*IEEE Micro* special issue. The invited authors then work hard to turn their slides into actual technical papers, which sometimes requires serious pruning. If you don't want to miss the extra details, and if you want a chance to question the authors directly, make sure you attend Hot Chips 20 in August 2008. Conferences come and go, but Hot Chips maintains its popularity!

For this issue, we've selected five papers to cover a broad range of topics.

### **Low-power mobile**

Jonathan Owen and Maurice Steinman present "Northbridge Architecture of AMD's Griffin Microprocessor Family" AMD's next-generation mobile processor, focusing especially on a new mobile-optimized northbridge design. Mobile designs demand difficult trade-offs between performance wishes, power consumption, and thermal constraints. In addition, when using a unified memory architecture for graphics, the northbridge has to handle the differing needs of graphics and CPU access to the same shared memory, and the display must be refreshed even when the CPU is idle.

### **Very old, still new**

Charles Webb of IBM writes of "IBM z10: The Next-Generation Mainframe Microprocessor." The IBM z10 processor implements IBM z/Architecture, the current generation of mainframe instruction set architecture, upward-compatible all the way back to the IBM S/360, now over 40 years old. The 4.4-GHz, 994-million-transistor chip is not only an aggressive chip by any standard, but the architectural longevity issue is likely unique. One of the editors (JRM) fondly remembers his first IBM S/360 from 1967, a Model 50 with a 2-MHz clock, and perhaps 512 Kbytes of main memory. This architecture has come an incredible distance since the days we wrote masses of assembly code to save every precious byte of memory, but programs written then are still running today.

### **Fault-tolerant microprocessor**

In an interesting design strategy discussed in the Webb article, the z10 and Power6 design teams worked together, sharing

common parts of the design where possible. In our third article, "Fault-Tolerant Design of the IBM Power6 Microprocessor," Kevin Reick, Pia N. Sanda, Jeffrey W. Kellington, Michael Mack, Michael Floyd, and Daniel Henderson describe how they incorporated mainframe-class reliability, availability, and serviceability (RAS) features while still achieving 4.7-GHz operation in a 790-million-transistor chip.

### **New and very parallel**

After considering three instruction set architectures whose longevities range from 15 to 40+ years, we switch to one that is rather new, as seen in "NVIDIA Tesla: A Unified Graphics and Computing Architecture," by Erik Lindholm, John Nickolls, Stuart Oberman, and John Montrym. For many years, 3D graphics processors have included multiple internal computing elements operating in parallel, but they were usually dedicated to running graphics code hidden behind graphics APIs. Tesla unifies the vertex and pixel processors and extends them so they are usable for more general applications, supported by the CUDA (Compute Unified Device Architecture) development tools. Given the high volumes in which such chips are shipped, it will be interesting to see the sorts of parallel applications that develop.

### **High-speed wireless at 60 GHz**

Finally, we recognize the importance of wireless communication these days. As representatives of the embedded side of the chip world, Jeffrey Gilbert, Chinh Doan, Sohrab Emami, and Bernard C. Shung of SiBEAM contribute "A 4-Gbps Uncompressed Wireless HD A/V Transceiver Chipset" Technologists around the world are working to exploit the wide unlicensed spectrum available at 60 GHz, and a leading candidate for using this bandwidth is high-data-rate, line-of-sight wireless data transmission. One potential consumer electronics application is streaming uncompressed HD video data directly to a display, which can then be made cheaper, lighter, and less power hungry by moving the video decoders from the display to the set-top box or media PC. This article

describes a chipset for enabling these links using smart antenna technology and implemented in conventional CMOS, a critical requirement for the low-cost consumer application space.

MICRO

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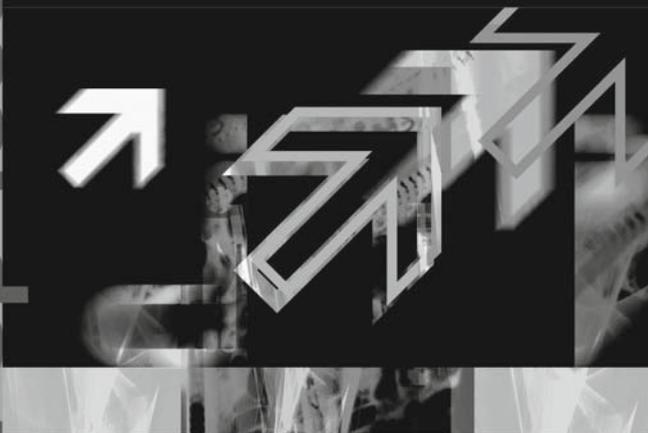
**John Mashey** is a consultant for venture capitalists and technology companies, and

he gives public talks on software engineering, RISC design, performance benchmarking, supercomputing, and Silicon Valley entrepreneurialism. Mashey was one of the founders of the SPEC benchmarking group, was an ACM National Lecturer for four years, and is one of the long-time organizers of Hot Chips. He holds a PhD in computer science from Pennsylvania State University.

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